the circuit diagram of which is shown in FIG. 7.

[FIG. 9] (a) through (d) are cross-sectional views of the linear device constituting the integrated circuit of the present invention shown in FIG. 8, respectively.

[FIG. 10] A perspective view of the integrated circuit of the present invention the circuit diagram of which is shown in FIG. 7.

[FIG. 11] A circuit diagram of a PLA constituted of an AND plane and an OR plane.

[FIG. 12] A perspective view of a linear device constituting the integrated circuit of the present invention the circuit diagram of which is shown in FIG. 11.

[FIG. 13] (a) and (b) are cross-sectional views of the linear device constituting the integrated circuit of the present invention shown in FIG. 12.

[FIG. 14] (a) is a circuit diagram of the AND plane of the PLA, and (b) is a perspective view of the integrated circuit of the present invention corresponding to the circuit diagram shown in (a).

[FIG. 15] (a) is a circuit diagram of the OR plane of the PLA, and (b) is a perspective view of the integrated circuit of the present invention corresponding to the circuit diagram shown in (a).

[FIG. 16] A perspective view of linear devices constituting a complementary MISFET of the present invention.

[FIG. 17] (a) through (f) are cross-sectional views

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